L Number	Hits	Search Text	DB	Time stamp
1	4968	((ready adj only adj memory) or EPROM or ROM) and (titanium or Ti) and (cobalt or Co)	USPAT; US-PGPUB	2004/09/16 10:15
2	1505	(((ready adj only adj memory) or EPROM or ROM) and (titanium or Ti) and (cobalt or Co)) and (silicon or polysilicon) and @ad<20020123	USPAT; US-PGPUB	2004/09/16 10:17
3	399	((((ready adj only adj memory) or EPROM or ROM) and (titanium or Ti) and (cobalt or Co)) and (silicon or polysilicon) and @ad<20020123) and silicide	USPAT; US-PGPUB	2004/09/16 11:28
4	377	(((((ready adj only adj memory) or EPROM or ROM) and (titanium or Ti) and (cobalt or Co)) and (silicon or polysilicon) and @ad<20020123) and silicide) and (remove or removing or etch or etching)	USPAT; US-PGPUB	2004/09/16 11:58
5	152	((((((ready adj only adj memory) or EPROM or ROM) and (titanium or Ti) and (cobalt or Co)) and (silicon or polysilicon) and @ad<20020123) and silicide) and (remove or removing or etch or etching)) and (cobalt adj silicide)	USPAT; US-PGPUB	2004/09/16 11:58
6	370	(((((ready adj only adj memory) or EPROM or ROM) and (titanium or Ti) and (cobalt or Co)) and (silicon or polysilicon) and @ad<20020123) and silicide) and (removed or etched)	USPAT; US-PGPUB	2004/09/16 11:58
8	0	(((((((ready adj only adj memory) or EPROM or ROM) and (titanium or Ti) and (cobalt or Co)) and (silicon or polysilicon) and @ad<20020123) and silicide) and (removed or etched)) and (cobalt adj silicide)) not ((((((ready adj only adj memory) or EPROM or ROM) and (titanium or Ti) and (cobalt or Co)) and (silicon or polysilicon) and @ad<20020123) and silicide) and (remove or removing or etch or etching)) and (cobalt adj silicide))	USPAT; US-PGPUB	2004/09/16 11:59
7	141	((((((ready adj only adj memory) or EPROM or ROM) and (titanium or Ti) and (cobalt or Co)) and (silicon or polysilicon) and @ad<20020123) and silicide) and (removed or etched)) and (cobalt adj silicide)	USPAT; US-PGPUB	2004/09/16 11:59

L Number	Hits	Search Text	DB	Time stamp
1	79	EPROM and cobalt and titanium and (cobalt adj silicide) and removing	USPAT; US-PGPUB	2004/09/09 16:09
2	54	(EPROM and cobalt and titanium and (cobalt adj silicide) and removing) and @ad<20020123	USPAT; US-PGPUB	2004/09/09 16:10
3	0	EPROM and cobalt and titanium and (cobalt adj silicide) and removing	EPO; JPO; DERWENT; IBM_TDB	2004/09/09 16:08
4	1	EPROM and cobalt and titanium and (cobalt adj silicide)	EPO; JPO; DERWENT; IBM_TDB	2004/09/09 16:08
5	119	EPROM and cobalt and titanium and (cobalt adj silicide)	USPAT; US-PGPUB	2004/09/09 16:10
6	79	(EPROM and cobalt and titanium and (cobalt adj silicide)) and @ad<20020123	USPAT; US-PGPUB	2004/09/09 16:10
7	25	((EPROM and cobalt and titanium and (cobalt adj silicide)) and @ad<20020123) not ((EPROM and cobalt and titanium and (cobalt adj silicide) and removing) and @ad<20020123)	USPAT; US-PGPUB	2004/09/09 16:10

US-PAT-NO: 6337245

DOCUMENT-IDENTIFIER: US 6337245 B1

TITLE: Method for fabricating flash memory device and flash
memory device fabricated thereby

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Assignee Name - ASNM (1):
Samsung Electronics Co., Ltd.

Assignee Group - ASGP (1):
Samsung Electronics Co., Ltd. Suwon KR 03

Brief Summary Text - BSTX (5):
A unit cell of a flash memory device has the same structure as that of a memory cell of an erasable programmable ROM (EPROM) device or an electrically erasable and programmable ROM (EEPROM) device. In other words, a flash memory cell includes a tunnel oxide film, a floating gate, an inter-gate dielectric film, and a control gate electrode serving as a word line, which are sequentially stacked on a channel region.

Brief Summary Text - BSTX (14):
As a result of this, the inter-gate dielectric film 9, which is exposed after the second conductive layer is etched, should be over etched. This results in a recess of the device isolation film 3 exposed between the plurality word lines WL.sub.1, WL.sub.2, . . . , and WL.sub.n, as shown in FIG. 3B, thereby reducing the thickness of the device isolation film 3. Of course, the recess phenomenon in the device isolation film

3 becomes more
serious as the first conductive layer pattern 7 becomes thicker, requiring
greater **etching to remove**.

Brief Summary Text - BSTX (29):
The forming of the plurality of word lines may comprise forming a
polysilicon film over portions of the semiconductor substrate from which the
isolated capping layers have been removed, forming a plurality of polysilicon
patterns insulated by the inter-gate dielectric film over the floating gate and
the device isolation film adjacent to the floating gate by blanket-etching the
polysilicon film until the insulating film pattern is exposed, wherein the
plurality of polysilicon patterns are formed in parallel in a direction in
which the plurality of polysilicon patterns cross the device isolation film,
and selectively forming a refractory metal **silicide** film over the plurality of
polysilicon patterns.

Detailed Description Text - DETX (16):
An inter-gate dielectric film 41 and a conductive layer 43 are then
sequentially formed over the entire surface of the semiconductor substrate
having the doped string selection line SSL, ground selection line GSL and
floating gate FG. It is preferable that the inter-gate dielectric film 41 be
formed of an oxide/nitride/oxide (O/N/O) film and that the conductive layer 43
be formed of a refractory metal polycide film comprising a polysilicon film and
a refractory metal **silicide** film such as a tungsten **silicide** film.

Detailed Description Text - DETX (23):
Referring to FIGS. 12A through 12C, the doped polysilicon film 101 is

blanket etched until the insulating film patterns 37 are exposed, thereby
forming a plurality of polysilicon patterns 101' over regions between the
insulating film patterns 37. Each polysilicon pattern 101' crosses the device
isolation film 23 and the active region. A refractory metal **silicide** film 103,
e.g., a **titanium silicide** film or a **cobalt silicide** film, is then selectively
formed over only the surface of the plurality of polysilicon patterns 101'.

Detailed Description Text - DETX (24):

Preferably this done through the use of a general salicide process, i.e., a
self-aligned **silicide** process. The general salicide process of forming the
refractory metal **silicide** film 103 will now be specifically described.
Primarily, a refractory metal film, e.g., a **titanium (Ti)** film or a **cobalt (Co)**
film, is formed over the entire surface of the semiconductor substrate having
the polysilicon pattern 101'. The refractory metal **silicide** film 103, e.g.,
the **titanium silicide** film or the **cobalt silicide** film is then formed
selectively over only the surface of the plurality of polysilicon patterns
101', preferably by thermal-processing the semiconductor substrate having the
refractory metal film. Unreacted refractory metal that remains on the surface
of the insulating film pattern 37 is then removed with a chemical solution.

Detailed Description Text - DETX (25):

The polysilicon pattern 101' and the refractory metal **silicide** film 103
formed over the string selection line SSL comprise a string gate line 105S.
The polysilicon pattern 101' and the refractory metal suicide film 103 formed
over the ground selection line GSL comprise a ground gate line 105G. The

polysilicon patterns 101' and the refractory metal **silicide** films 103 running
over the floating gates FG comprise a plurality of word lines W.sub.1,
WL.sub.2, . . . , and WL.sub.n.

Detailed Description Text - DETX (26):
Referring to FIGS. 13A through 13C, the interlayer insulating film 45
described in the first preferred embodiment of the present invention is formed
over the entire surface of the semiconductor substrate, including the
refractory metal **silicide** film 103. Then, a contact hole exposing the bit line
contact region BC and first and second bit lines BL.sub.1 and BL.sub.2 is
formed by the same method as used in the first preferred embodiment of the
present invention. In the second preferred embodiment, however, a word line
that is self-aligned with each floating gate can be formed.

Claims Text - CLTX (26):
selectively forming a refractory metal **silicide** film over the plurality of
polysilicon patterns.